What is Claimed is:

[c1] A ring oscillator comprising an odd number of elements interconnected in a serially-connected infinite loop, each said element having an associated programmable delay.

[c2] The ring oscillator of claim 1, further comprising:

an input to receive an input signal to start an oscillation of said ring oscillator.

[c3] The ring oscillator of claim 1, further comprising:

an input to receive an input signal to program each said programmable delay.

[c4] The ring oscillator of claim 1, wherein each said element comprises a non-inverting amplifier.

[c5] The ring oscillator of claim 1, wherein said input for said programmable delay provides an adjustment of a duty factor of an output signal of said ring oscillator.

[c6] The ring oscillator of claim 1, wherein each said element comprises at least one complementary metal oxide semiconductor (CMOS) inverter.

[c7] The ring oscillator of claim 3, wherein said programmable delay comprises a binary word serving as a vector input.

[c8] A circuit for testing effects of Negative Bias Temperature Instability (NBTI) on an integrated circuit, said circuit comprising: a ring oscillator according to claim 1.

[c9]

A test circuit to measure a Negative Bias Temperature Instability (NBTI) effect for PFETs (p-channel MOSFET) by stressing a target PFET component with at least one stress condition, said target PFET component being integrated as a component into said test circuit, said target PFET component having a source, a drain, and a gate, said test circuit comprising:

a ring oscillator comprising an odd number of oscillator elements interconnected serially in an infinite loop, wherein at least one said target

PFET component is integrated into said ring oscillator; and

a test output providing a point to measure at least one parameter of said ring oscillator.

[c10] The NBTI test circuit of claim 9, wherein each said oscillator element contains at least one said target PFET.

[c11] The NBTI test circuit of claim 9, further comprising:

a switching circuit to selectively switch said at least one stress condition onto said target PFET.

[c12] The NBTI test circuit of claim 11, wherein said at least one stress condition comprises at least one of:

a DC stress, wherein said target PFET receives a first constant voltage level on said gate and a second constant voltage level on said source and drain;

an AC stress, wherein said target PFET receives a varying voltage on said gate; and

a free running mode, wherein said target PFET receives a varying complementary voltage on said drain and said gate.

[c13] The NBTI test circuit of claim 11, wherein said target PFET is stressed by an AC stress by selectively applying a gate pulse, said gate pulse being adjustable in at least one of frequency and duty factor.

[c14] A method of testing a PFET (p-channel field effect transistor), comprising:

incorporating a target PFET into a ring oscillator having an odd number of elements;

performing at least one stress test on said PFET; and

measuring at least one characteristic of said ring oscillator.

[c15] The method of claim 14, wherein said each said ring oscillator element contains a variable delay.

[c16] The method of claim 14, wherein said test measurement determines an NBTI (negative bias temperature instability) effect on at least one said target PFET.

[c17] The method of claim 14, wherein said test measurement is for adjusting a design of MOSFET devices, said method further comprising: systematically performing at least one stress test on said target PFET; and

taking at least one measurement of each said at least one stress test; and

using said at least one measurement to modify a design parameter of said target PFET.

[c18] The method of claim 17, wherein said design parameter is used for at least one of correcting a manufacturing process and improving a design characteristic.

[c19] The method of claim 14, wherein said test is for one of predicting and improving a reliability of one or more MOSFET devices having a structure similar to said target PFET.v

[c20] The method of claim 14, wherein said test is for one of predicting and improving a degradation over time of one or more MOSFET devices similar to said target PFET.